CS 250 Fall 2017 Homework 03

Due 11:58pm Thursday, SEPTEMBER 14, 2017

Submit your typewritten file in PDF format to Blackboard.

1. How can an S’R’ latch be made to emit a falling edge on its output Q?

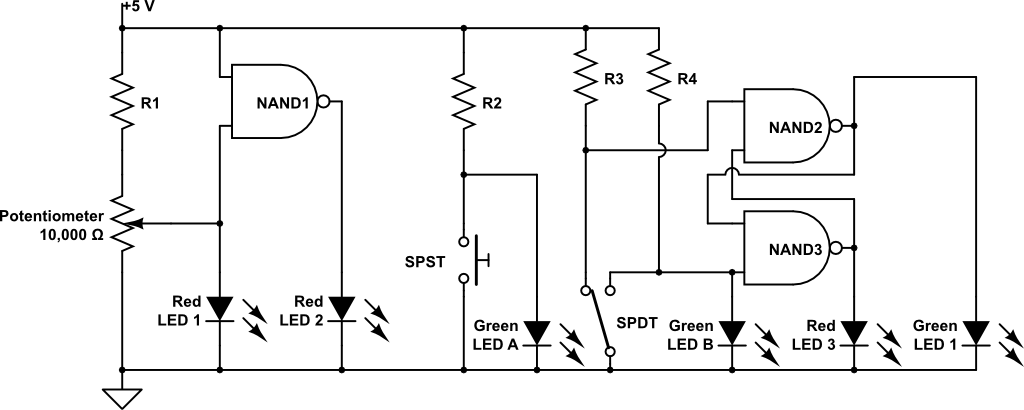
We can make S’ = 1 and R’= 0 and reset it and it will give a falling edge

1. Imagine that the 74163 rising-edge-triggered counter chip is being clocked with an SR latch, the same as in Lab 02.
   1. What is the shortest sequence of Set and Reset operations that will advance the count from 14 to 1? Use S to mean set and R to mean reset and write your answer in the form of an ASCII character string.

RSRSRS

* 1. Extra thought: Using a regular expression, describe all sequences of Set and Reset that will drive the count from 14 to 1.

{RSRSRS, (RSRSRSRSRSRSRSRSRSRSRSRSRSRSRSRSRSRSRS)\*}

1. Consider the schematic below for the following questions. The difference between this circuit and the circuit of Lab 02 is that the 74163 counter has been removed.   
     
   1. Which LED shows that it is possible to operate LEDs at half brightness rather than just fully off or fully on. Be sure to use the exact name shown in the schematic so that there is no ambiguity in your answer.

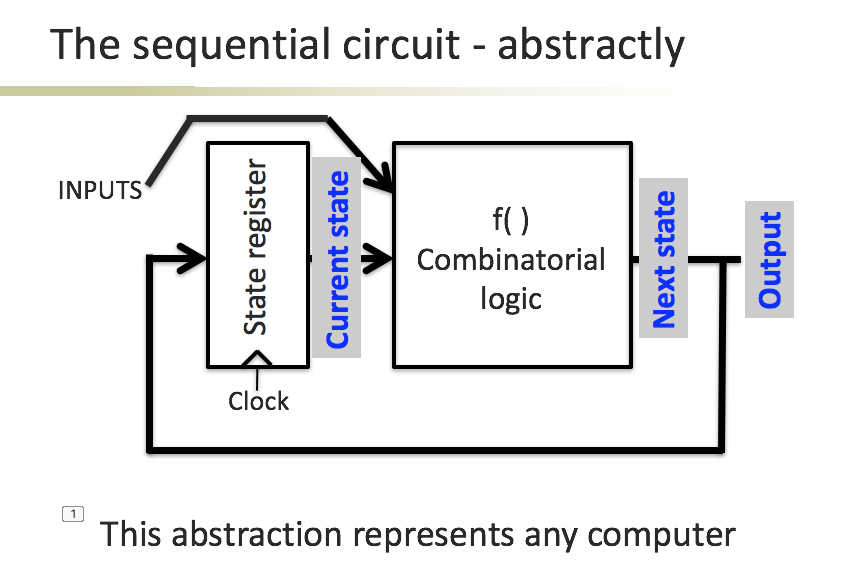
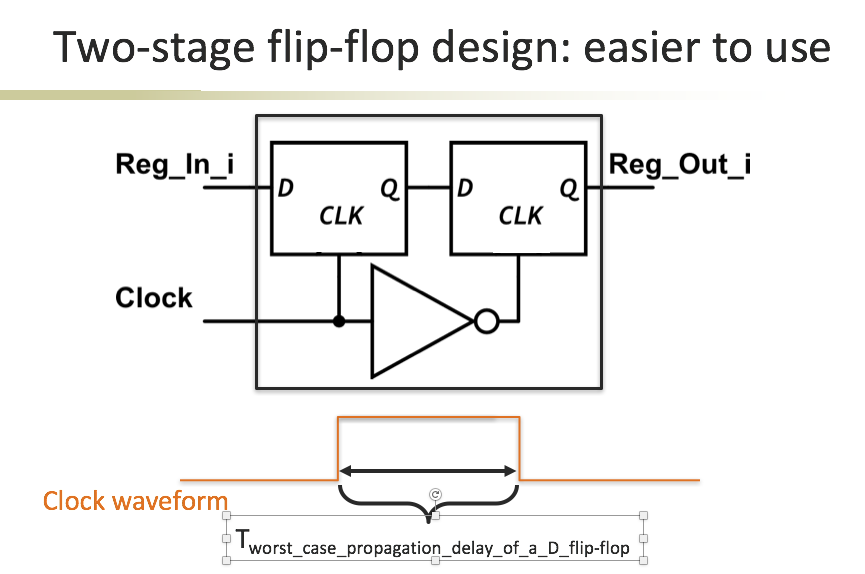
**Answer:** Red LED 1

* 1. Name all LEDs in the schematic above that are connected to de-bounced clock signals. If no such LED exists, write “None.” Be sure to use the exact name shown in the schematic so that there is no ambiguity in your answer.

**Answer:** Red LED3 & Green LED1

* 1. Let Red LED3 be the Q’ output of the S’R’ latch formed by NAND2 and NAND3. The moving pole of the SPDT switch has three positions: connected to R3 (R3, for a short name), in between the R3 and R4 contacts (B, for a short name) where the pole is connected to nothing, and connected to R4 (just called R4). Fill in the five missing entries in the following table for each time step from 0 to 5.

|  |  |  |
| --- | --- | --- |
| Time | SPDT position | Red LED 3 state |
| 0 | R3 | OFF |
| 1 | R3 | **OFF** |
| 2 | B | **OFF** |
| 3 | R4 | **ON** |
| 4 | B | **ON** |
| 5 | **R3** | OFF |

1. A sequential circuit is modeled shown here (from lecture slides).   
     
     
   There is a feedback loop in this circuit that links the Current state output from the State register to the input of the State register. Let the State register be built using the two-stage flip-flop design shown here.  
     
     
   What is the minimum time between presenting a new “Current state” on the output wires of the State register and presenting a new current state, the “Next state” on those same output wires, Tminimum\_Current\_state\_to\_Next\_state?

2\*Tworst case propagation delay of a D flip flop + Tminimum of combinatorial circuit

1. What is the minimum number of gates required to construct a 5x32 decoder? What is the worst case propagateion delay for the decoder in units of gate delays? How does this compare to the number of gates needed to build a 5-bit ripple-carry adder, an adder that accepts inputs represented using 5 bits, and to the worst case propagation delay adder? What is the ratio of speed decoder to adder?

5x32 decoder needs 5 NOT gates and 32 AND gates. Worst case propagation delay for the decoder is 6 units. Ripple carry adder needs more gates. Worst case propagation delay for the 5 bits’ adder is 2(5) +2 = 12 units which is more than the delay for the decoder. Ration of the speed decoder to adder is 6/12 = 0.5